28.1 A 5V AC-Powered CMOS Filter-Selectivity Booster for POTS/ADSL Splitter Size Reduction

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POTS/ADSL splitters separate the voice-band signal (300Hz to 3.4kHz) from the ADSL signal (30kHz to 2.2MHz) and are needed at the central office as well as the customer premises. The splitter is implemented with an HPF, typically integrated with the ADSL modem, and an LPF, the so-called POTS filter. Currently, POTS filters are implemented as passive L-C filters using several large transformers per phone line. To reduce the space taken up by the POTS-filter shelves in the central office, there is great interest in replacing these POTS filters with smaller active circuits [1].

One difficulty with an active implementation is that it has to withstand large ringing voltages (>200V), large ADSL voltages ($40V_{PP}$), as well as high common-mode voltages. The active-filter chip is preferably implemented in a low-voltage CMOS technology and should consume <50mW. In [1] a line-powered solution requiring 2 chips and 1 transformer per line has been reported. In this paper, an externally-powered solution is presented, where an active circuit boosts the selectivity of a passive single-transformer L-C filter. This approach needs one CMOS chip per line and avoids chips in series with the phone line, thus guaranteeing uninterrupted phone service even when the chip or its power fails.

Figure 28.1.1 shows the single-ended concept of the active POTS filter with the booster chip. At first ignoring R_S, C_S, the chip, and grounding node x, the circuit presents a passive single-inductor LPF (C_M, L, C_E, and C_H, where C_H is part of the HPF portion of the splitter), which rolls off at about 60dB/dec and has a null due to the resonance of L and C_E. This roll off is not sufficient to meet the POTS-band insertion loss (< 0.3dB) and ADSL-band isolation (> 65dB) specifications. Now activating the chip, the roll off is improved to about 140dB/dec. The boosted filter response has a total of 3 nulls, of which the lower 2 are active and the highest one is passive. The AC-coupled chip is protected from high ringing voltages by the HPF R_S, C_S and from large ADSL voltages by the inductor L.

Figure 28.1.2 shows the fully differential implementation of the booster concept and a block diagram of the chip. In order to protect the chip from large common-mode voltages on the line, it is powered by a floating supply. A transformer supplying 5V AC at 500kHz powers the chip through an on-chip low-voltage-drop active rectifier. An external capacitor (C_F) is needed to remove ripple from the DC voltage. The chip contains a 5^{th}-order continuous-time R-C filter with class-AB opamps. PVT variations are calibrated out with switched-capacitor arrays in the filter and a mixed-signal calibration engine similar to [2]. The calibration is performed relative to a precise 500kHz clock derived from the AC supply. The on-chip filter is followed by a class-AB driver that is able to drive large capacitive loads ($2C_M$ = 120nF) and has a low output resistance (<2.5Ω per side) up to high frequencies to insure good ADSL-band isolation of the POTS filter.

As shown in Fig. 28.1.3, the driver consists of an output driver and a predriver providing the necessary loop gain to obtain the low output resistance. To make the driver stable for large capacitive loads and keep the output resistance low up to high frequencies, the predriver pole is placed at a high frequency and the output-driver pole is placed at a low frequency, i.e, the reverse pole ordering of a classical 2-stage opamp is used. To ensure stability, a minimum load capacitance (C_L, C_L' = 10nF) is required.

The folded-cascode predriver stage in Fig. 28.1.3 uses NMOS loads (M_2, M_2', M_3, M_3'), that track the NMOS input transistors (M_1, M_1'), to provide a well-controlled gain. Too little gain cannot provide the required low output resistance and too much gain makes the driver unstable. The difference in size of M_2 and M_3 (M_2' and M_3') determines the gain while the sum determines the output common-mode voltage. Clamps (M_4, M_4') further stabilize the gain under large-signal conditions. Gate resistors (R_1, R_1', R_2, R_2') introduce a zero to increase the predriver bandwidth, i.e., to minimize the open-loop phase shift at high frequencies, thus improving the phase margin and the stability of the driver.

Figure 28.1.4 shows the class-AB output driver. The circuit M_1-M_3 and M_1'-M_3' transfers the differential input voltage to the ground-referred nodes x and y. Current sources I_1 and I_1' set the quiescent current for the output transistors M_5 and M_6. A current limiter (M_4, M_4', M_4”) clamps the voltages at nodes x and y to the reference voltage V_{Lim}.

Figure 28.1.5 shows the on-chip active full-wave rectifier. Each of the 4 diodes is realized with a MOS transistor controlled by a voltage comparator such that the transistor turns on when the diode is forward biased. The width of the transistors is chosen such that the forward voltage drop is limited to about 0.1V. Note that the parasitic drain/substrate and drain/n-well junction diodes form a passive rectifier in parallel with the active one, which helps the start-up process. At power up, the passive rectifier produces a dc voltage of about V_{AC}-1.4V, which is sufficient to power up the comparators. Then, the active rectifier becomes operational boosting the dc voltage to about V_{AC}-0.2V. The switch transistors are guard ringed to avoid latch-up during start-up.

Figure 28.1.6 shows measurement results of the POTS filter. The solid curve shows the frequency response of the active POTS filter; the dashed curve shows the response of the passive network for comparison. The chip boosts the ADSL isolation from about 45dB to well over 70dB at 30kHz. Simultaneously, the passband flatness is improved from about 0.4dB (passive) to 0.23dB (active). The chip operates at 5V and consumes a quiescent current of 7mA (P = 35mW). The on-chip rectifier is measured separately and has a power efficiency of 89% when supplying an output current of 10mA.

Figure 28.1.7 shows the chip, which is fabricated in a 5V 0.5μm CMOS technology and occupies an area of 2.4×2.4 mm² (including test pads and test circuits).

References:
[1] H. Dedieu, et al., “7th-Order Low-Voltage CMOS POTS/ADSL Splitter for DSL Access Multiplexer Size Reduction,” *ISSCC Dig. Tech. Papers*, pp. 408-409, Feb., 2004.
[2] Anna M. Durham and William Redman-White, “Integrated Continuous-Time Balanced Filters for 16-b DSP Interfaces,” *IEEE J. Solid-State Circuits*, vol. 28, pp. 835-839, July, 1993.

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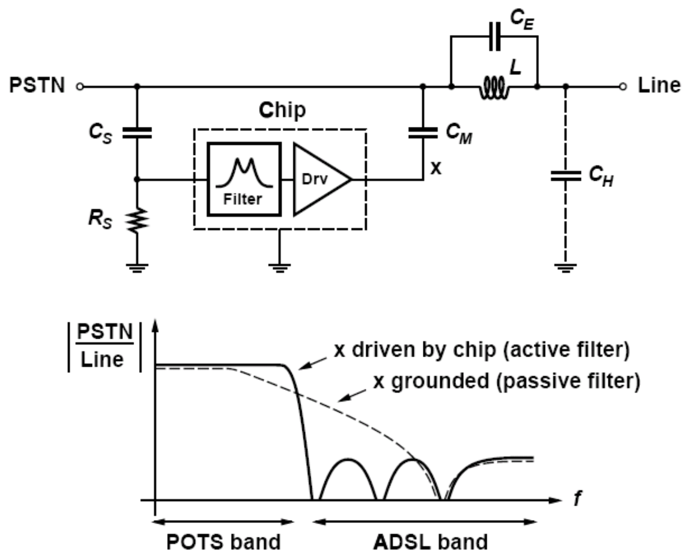

Figure 28.1.1: L-C filter with selectivity booster chip.

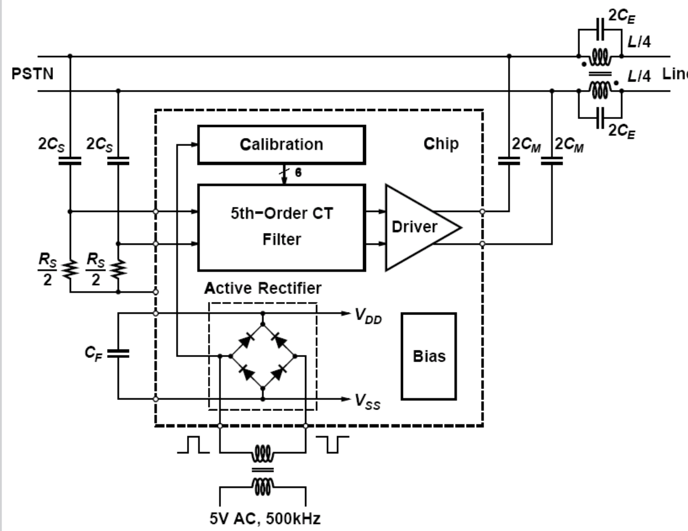

Figure 28.1.2: Block diagram of the chip with external components.

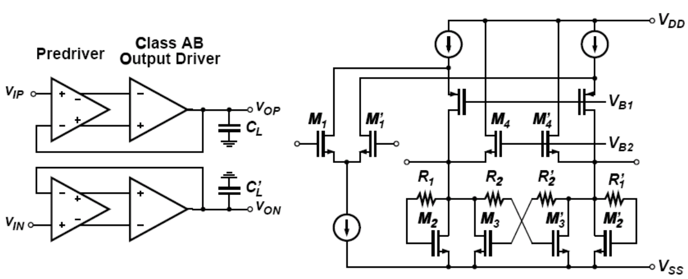

Figure 28.1.3: Driver architecture and predriver circuit.

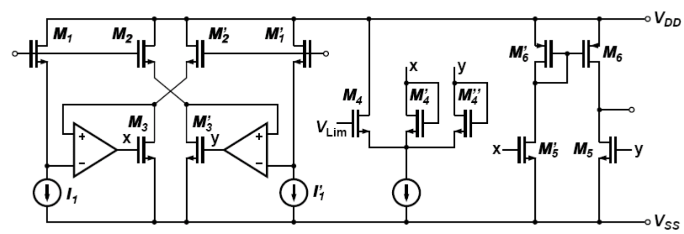

Figure 28.1.4: Class-AB output driver with current limiter.

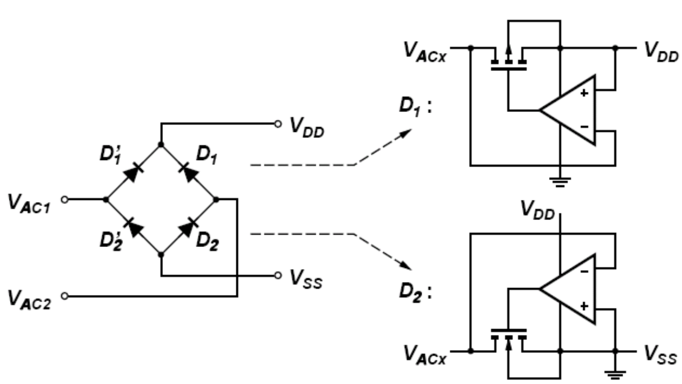

Figure 28.1.5: Active rectifier.

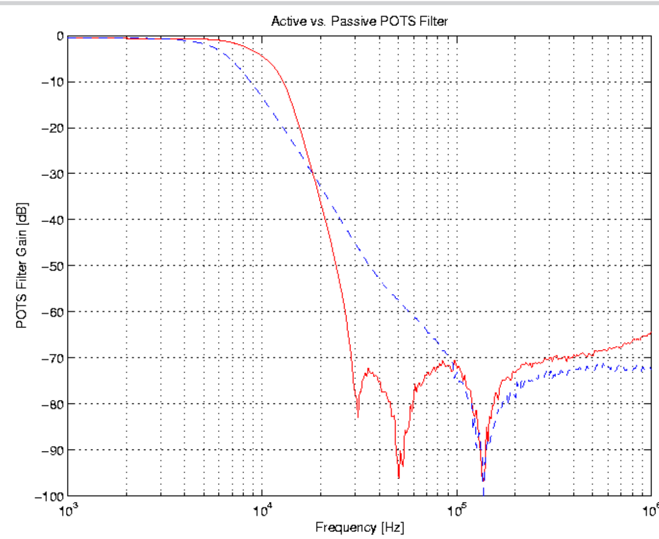

Figure 28.1.6: Measured frequency response of active (solid) and passive (dashed) POTS filter.

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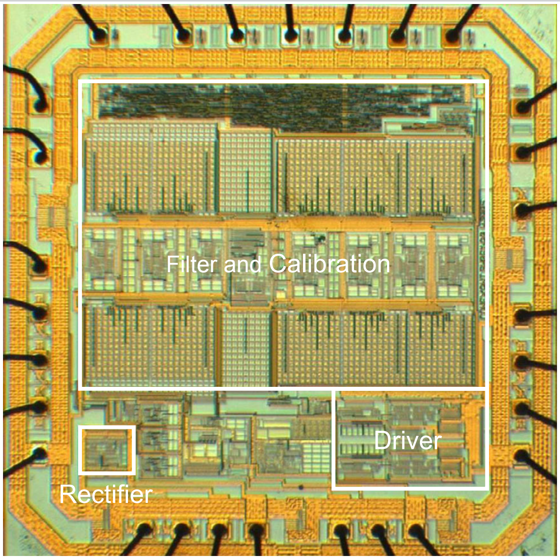

Figure 28.1.7: Chip micrograph.